What is claimed is:

1. A ferroelectric memory device comprising:

a memory cell array in which memory cells are arranged in a matrix, the memory cell array including first signal electrodes, second signal electrodes arranged in a direction intersecting the first signal electrodes, and a ferroelectric layer disposed at least in intersection regions between the first signal electrodes and the second signal electrodes; and

a peripheral circuit section for selectively writing information into or reading information from the memory cell,

wherein the memory cell array and the peripheral circuit section are disposed in different layers, and

wherein the peripheral circuit section is formed in a region outside the memory cell array.

2. The ferroelectric memory device according to claim 1,

wherein the ferroelectric layer is disposed linearly along the first signal electrodes or the second signal electrodes.

3. The ferroelectric memory device according to claim 2,

wherein the ferroelectric layer is selectively disposed over the first signal electrodes.

4. The ferroelectric memory device according to claim 3,

wherein the memory cells are disposed over a base, and a dielectric layer is provided between laminates formed of the

first signal electrodes and the ferroelectric layer so as to cover exposed areas of the base.

5. The ferroelectric memory device according to claim 4, wherein the dielectric layer is formed of a material having a dielectric constant lower than a dielectric constant of the ferroelectric layer..

6. The ferroelectric memory device according to claim 4, wherein a surface-modifying layer having a surface characteristic differing from a surface characteristic of a surface of the base is formed over the base.

7. The ferroelectric memory device according to claim 6, wherein the surface-modifying layer is disposed in regions in which the memory cells are not formed and has a surface exhibiting weaker affinity to a material which forms the memory cells than a surface of the base.

8. The ferroelectric memory device according to claim 6, wherein the surface-modifying layer is disposed in regions in which the memory cells are formed and has a surface exhibiting stronger affinity to a material which forms the memory cells than a surface of the base.

9. The ferroelectric memory device according to claim 2, wherein the ferroelectric layer is selectively disposed

under the second signal electrodes.

10. The ferroelectric memory device according to claim 9, wherein the memory cells are disposed over a base, and a dielectric layer is provided between laminates formed of the ferroelectric layer and the second signal electrode so as to cover exposed areas of the base and the first signal electrodes.

11. The ferroelectric memory device according to claim 9, wherein the dielectric layer is formed of a material having a dielectric constant lower than a dielectric constant of the ferroelectric layer.

12. The ferroelectric memory device according to claim 2, wherein the ferroelectric layer is disposed only in the intersection regions between the first signal electrodes and the second signal electrodes.

13. The ferroelectric memory device according to claim 12, wherein the memory cells are disposed over a base, and a dielectric layer is provided between laminates formed of the first signal electrodes and the ferroelectric layer so as to cover part of exposed areas of the base.

14. The ferroelectric memory device according to claim 13, wherein the exposed areas of the base and the first signal electrodes are covered with the dielectric layer over the base.

15. The ferroelectric memory device according to claim 13, wherein the dielectric layer is formed of a material having a dielectric constant lower than a dielectric constant of the ferroelectric layer.

16. The ferroelectric memory device according to claim 13, wherein a surface-modifying layer having a surface characteristic differing from a surface characteristic of a surface of the base is formed over the base.

17. The ferroelectric memory device according to claim 16, wherein the surface-modifying layer is disposed in regions in which the memory cells are not formed and has a surface exhibiting weaker affinity to a material which forms the memory cells than a surface of the base.

18. The ferroelectric memory device according to claim 16, wherein the surface-modifying layer is disposed in regions in which the memory cells are formed and has a surface exhibiting stronger affinity to a material which forms the memory cells than a surface of the base.

19. The ferroelectric memory device according to claim 1, further comprising:

an insulating base,

wherein the memory cell array comprises the first signal

electrodes provided in grooves formed in the insulating base, the ferroelectric layer, and the second signal electrodes, and

wherein the ferroelectric layer and the second signal electrodes are layered over the insulating base in which the first signal electrodes are formed.

20. The ferroelectric memory device according to claim 1,

wherein the memory cell array comprises an insulating base,

wherein depressed sections and projected sections are provided to the insulating base in a given pattern,

wherein the first signal electrodes are disposed at a bottom of the depressed sections and on the upper surface of the projected sections, and

wherein the ferroelectric layer and the second signal electrodes are stacked over the insulating base over which the first signal electrodes are formed.

21. A ferroelectric memory device comprising a plurality of unit blocks of the ferroelectric memory device as defined in claim 1 arranged in a given pattern.

22. The ferroelectric memory device according to claim 1, comprising:

a plurality of memory cell arrays,

wherein the plurality of memory cell arrays is layered.

23. The ferroelectric memory device according to claim 1,

wherein insulation layers are provided between the first signal electrodes, and

wherein upper surfaces of the first signal electrodes are on the same level as upper surfaces of the insulation layers.

24. A method of manufacturing a ferroelectric memory device, comprising steps of:

(a) forming a peripheral circuit section for selectively writing information into or reading information from the memory cell over a semiconductor substrate; and

(b) forming at least first signal electrodes, second signal electrodes arranged in a direction intersecting the first signal electrodes, and a ferroelectric layer disposed at least in intersection regions between the first signal electrodes and the second signal electrodes, and forming a memory cell array in which memory cells are arranged in a matrix,

wherein the peripheral circuit section is formed in a region outside the memory cell array.

25. The method of manufacturing a ferroelectric memory device according to claim 24,

wherein the step (b) comprises steps of:

(b-1) forming the first signal electrodes;

(b-2) forming the ferroelectric layer; and

(b-3) forming the second signal electrodes.

26. The method of manufacturing a ferroelectric memory device according to claim 25,

wherein the step (b-2) comprises a step of forming an amorphous ferroelectric layer or a microcrystalline ferroelectric layer, and a step of forming the ferroelectric layer by subjecting the amorphous ferroelectric layer or the microcrystalline ferroelectric layer to a heat treatment.

27. The method of manufacturing a ferroelectric memory device according to claim 25,

wherein the step (b-2) is a step of forming the ferroelectric layer linearly along the first signal electrodes.

28. The method of manufacturing a ferroelectric memory device according to claim 27, further comprising:

a step of forming, over a base, a first region having a surface characteristic which causes a material for forming at least one of the first signal electrodes or the ferroelectric layer to be deposited preferentially, and a second region having a surface characteristic which causes a material for forming at least one of the first signal electrodes or the ferroelectric layer to be less deposited than the first region; and

a step of providing a material for forming at least one of the first signal electrodes or the ferroelectric layer and selectively forming the material in the first region.

29. The method of manufacturing a ferroelectric memory device

according to claim 28,

wherein the first region and the second region are formed on a surface of the base.

30. The method of manufacturing a ferroelectric memory device according to claim 29,

wherein a surface of the base is exposed in the first region, and

wherein a surface-modifying layer that has a surface characteristic exhibiting weaker affinity to the material for forming the first signal electrodes and the ferroelectric layer than the exposed surface of the base in the first region is formed in the second region.

31. The method of manufacturing a ferroelectric memory device according to claim 29,

wherein a surface of the base is exposed in the second region, and

wherein a surface-modifying layer that has a surface characteristic exhibiting stronger affinity to the material for forming the first signal electrodes and the ferroelectric layer than the exposed surface of the base in the second region is formed in the first region.

32. The method of manufacturing a ferroelectric memory device according to claim 27,

wherein a dielectric layer is provided between laminates

formed of the first signal electrodes and the ferroelectric layer so as to cover exposed areas of the base.

33. The method of manufacturing a ferroelectric memory device according to claim 32,

wherein the dielectric layer is formed of a material having a dielectric constant lower than a dielectric constant of the ferroelectric layer.

34. The method of manufacturing a ferroelectric memory device according to claim 25,

wherein the ferroelectric layer and the second signal electrodes are formed in a direction intersecting the first signal electrodes, and

wherein the ferroelectric layer is formed linearly along the second signal electrodes.

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35. The method of manufacturing a memory cell array according to claim 34,

wherein the ferroelectric layer and the second signal electrodes are patterned by etching using the same mask.

36. The method of manufacturing a memory cell array according to claim 34,

wherein a dielectric layer is provided between laminates formed of the ferroelectric layer and the second signal electrode so as to cover exposed areas of the base and the first

signal electrodes.

37. The method of manufacturing a memory cell array according to claim 36,

wherein the dielectric layer is formed of a material having a dielectric constant lower than a dielectric constant of the ferroelectric layer.

38. The method of manufacturing a ferroelectric memory device according to claim 25, further comprising:

a step (b-4) of patterning the ferroelectric layer after the step (b-3), and causing the ferroelectric layer to remain in a shape of a block only in intersecting regions between the first signal electrodes and the second signal electrodes.

39. The method of manufacturing a ferroelectric memory device according to claim 38, further comprising:

a step of forming, over the base, a first region having a surface characteristic which causes a material for forming at least one of the first signal electrodes or the ferroelectric layer to be deposited preferentially, and a second region having a surface characteristic which causes a material for forming at least one of the first signal electrodes or the ferroelectric layer to be less deposited than the first region; and

a step of providing a material for forming at least one of the first signal electrodes or the ferroelectric layer and selectively forming the material in the first region.

40. The method of manufacturing a ferroelectric memory device according to claim 39,

wherein the first region and the second region are formed on a surface of the base.

41. The method of manufacturing a ferroelectric memory device according to claim 40,

wherein a surface of the base is exposed in the first region, and

wherein a surface-modifying layer that has a surface characteristic exhibiting weaker affinity to the material for forming the first signal electrodes and the ferroelectric layer than the exposed surface of the base in the first region is formed in the second region.

42. The method of manufacturing a ferroelectric memory device according to claim 40,

wherein a surface of the base is exposed in the second region, and

wherein a surface-modifying layer that has a surface characteristic exhibiting stronger affinity to the material for forming the first signal electrodes and the ferroelectric layer than the exposed surface of the base in the second region is formed in the first region.

43. The method of manufacturing a ferroelectric memory device

according to claim 38,

wherein the ferroelectric layer and the second signal electrodes are patterned by etching using the same mask.

44. The method of manufacturing a ferroelectric memory device according to claim 38,

wherein a dielectric layer is provided between laminates formed of the first signal electrodes and the ferroelectric layer so as to cover exposed areas of the base.

45. The method of manufacturing a ferroelectric memory device according to claim 44,

wherein a dielectric layer is provided between laminates formed of the ferroelectric layer and the second signal electrode so as to cover exposed areas of the base and the first signal electrodes.

46. The method of manufacturing a ferroelectric memory device according to claim 44,

wherein the dielectric layer is formed of a material having a dielectric constant lower than a dielectric constant of the ferroelectric layer.

47. The method of manufacturing a ferroelectric memory device according to claim 24, further comprising:

a step (b-5) of insulation layers between the first signal electrodes after the step (b-1),

wherein upper surfaces of the insulation layers are on the same level as upper surfaces of the first signal electrodes.

48. The method of manufacturing a ferroelectric memory device according to claim 47,

wherein the step (b-5) is a step of forming the insulation layers using a solution application process and planarizing the insulation layers.

49. An embedded device comprising:

the ferroelectric memory device as defined in any one of claims 1 to 23; and

at least one component selected from a group including a flash memory, a processor, an analog circuit, and an SRAM.